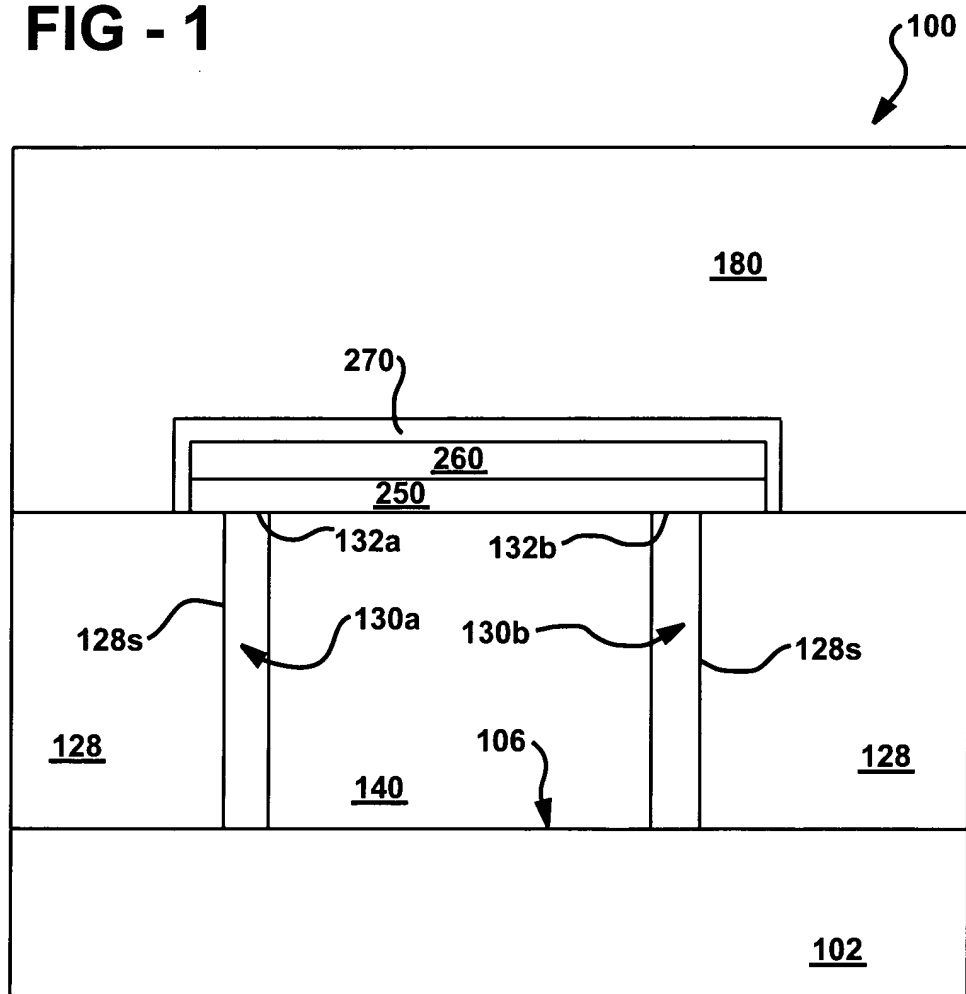


FIG - 1



[illegible]

FIG - 3

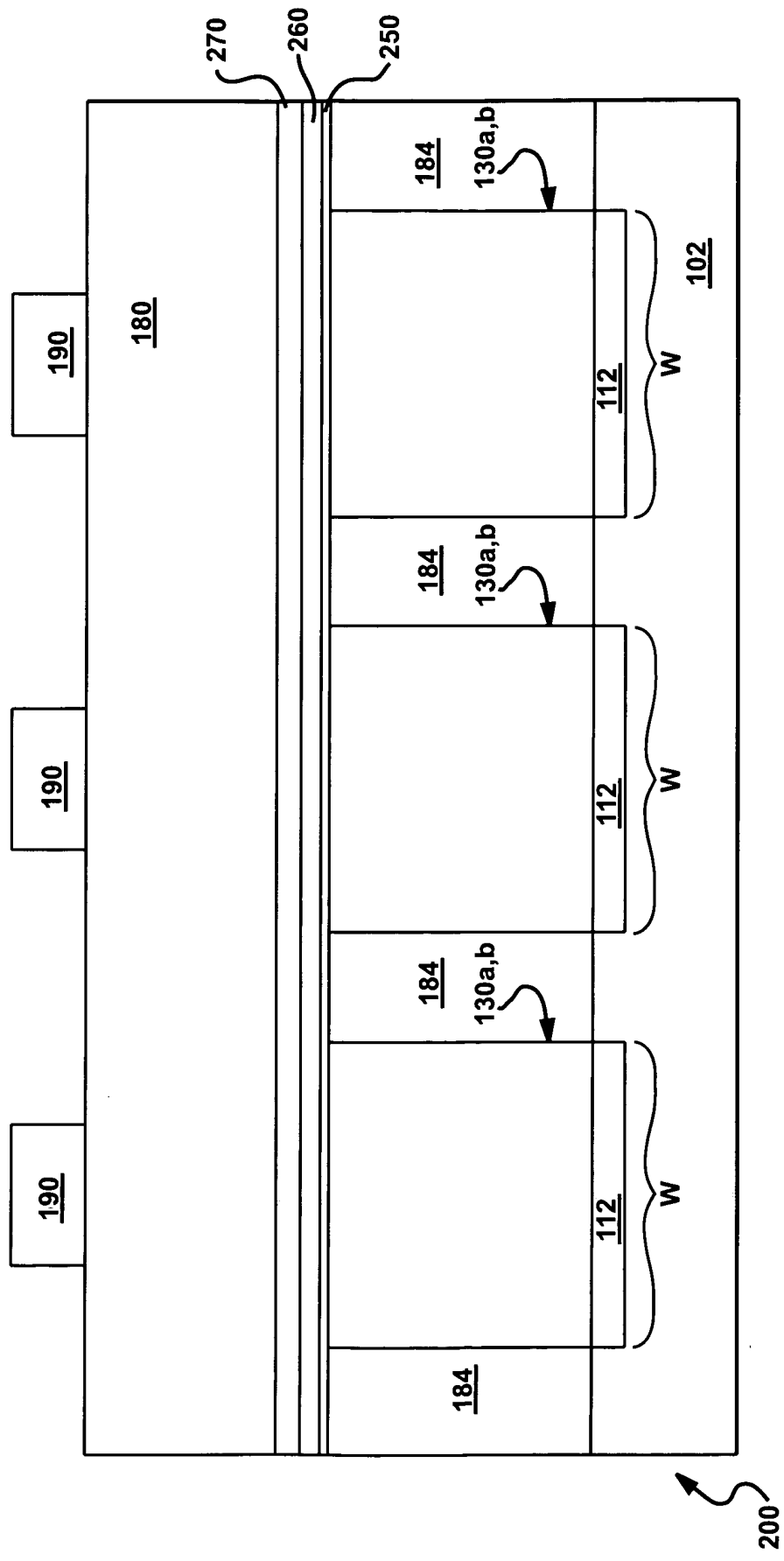


FIG - 4

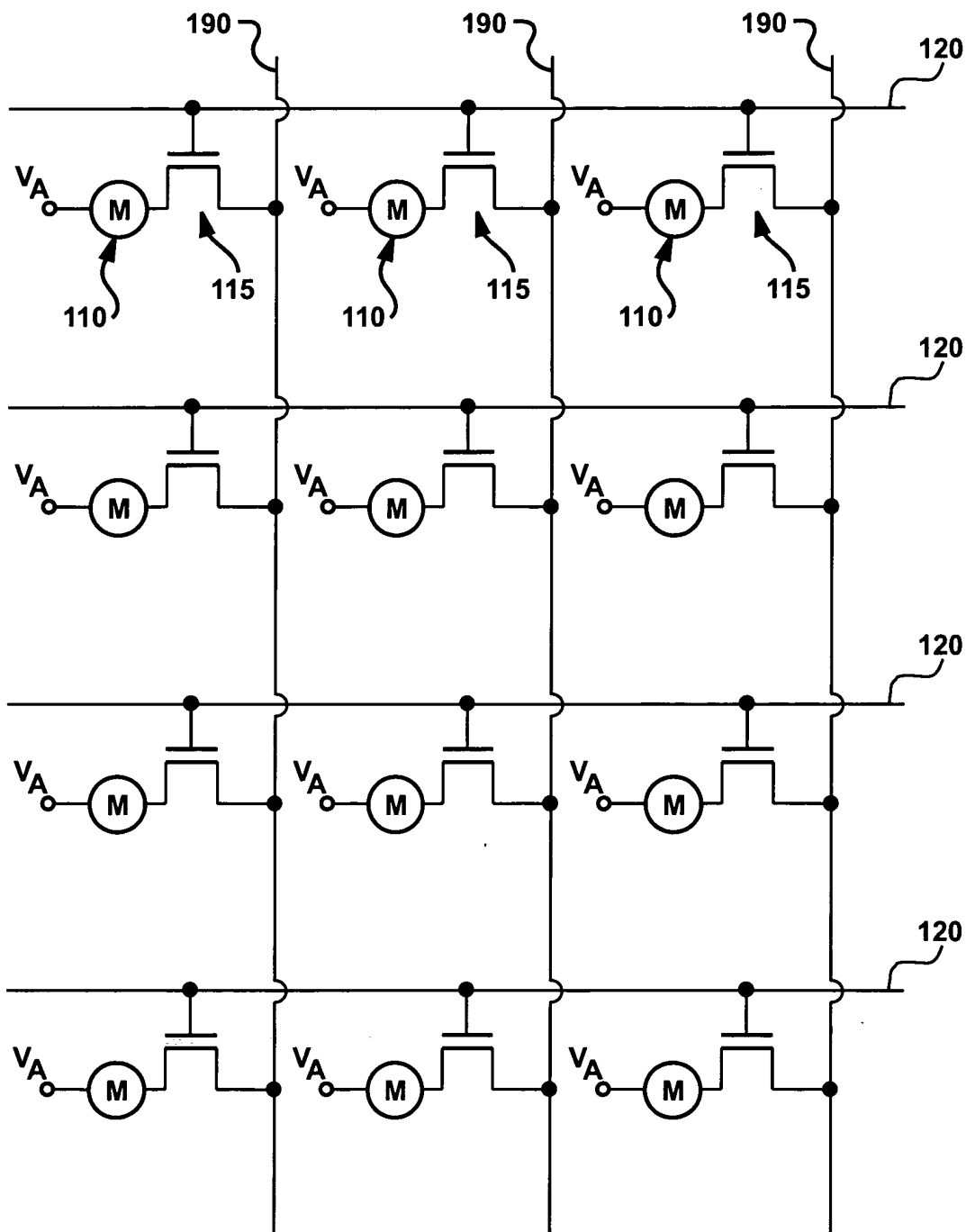


FIG - 5A

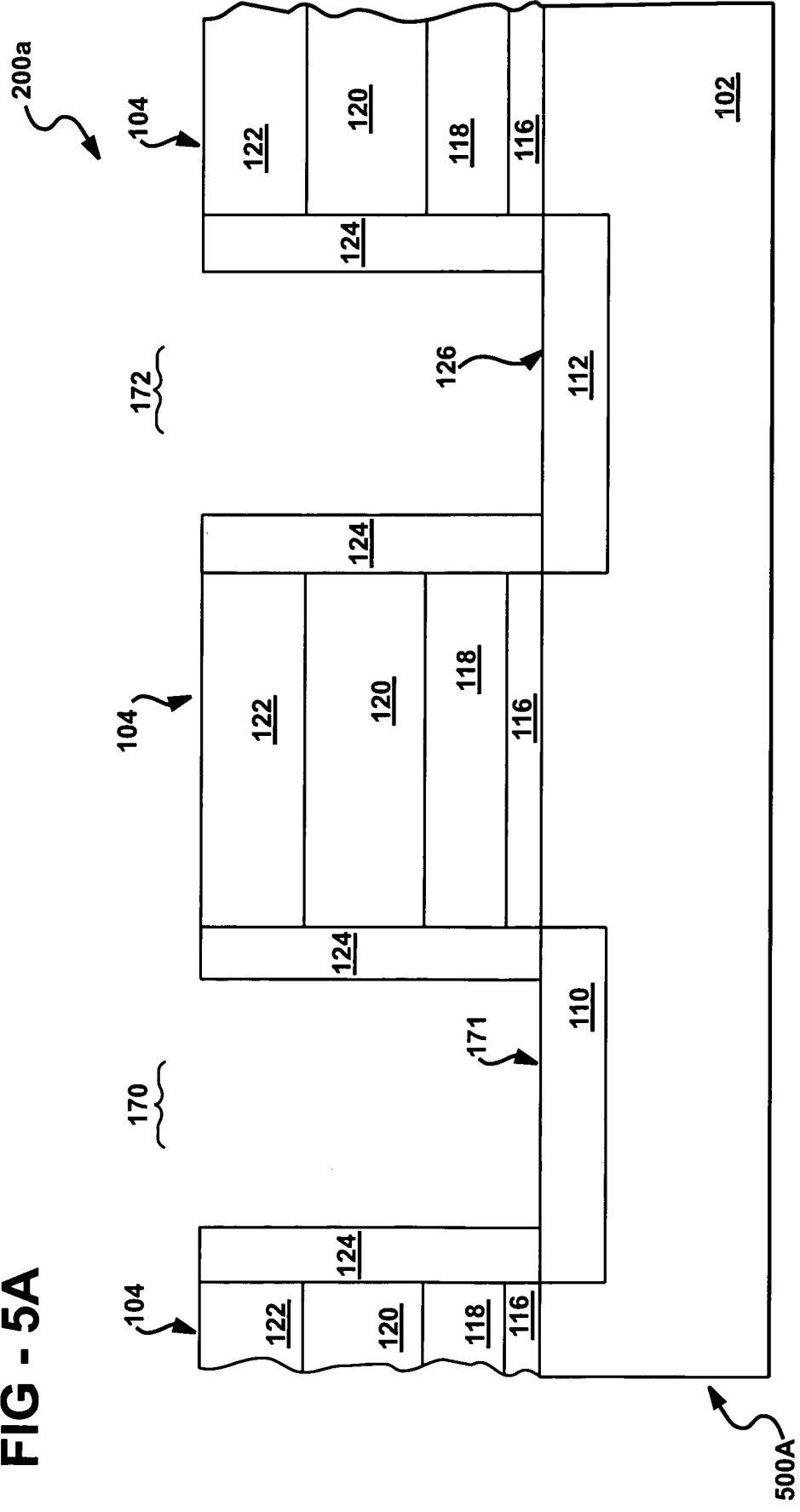
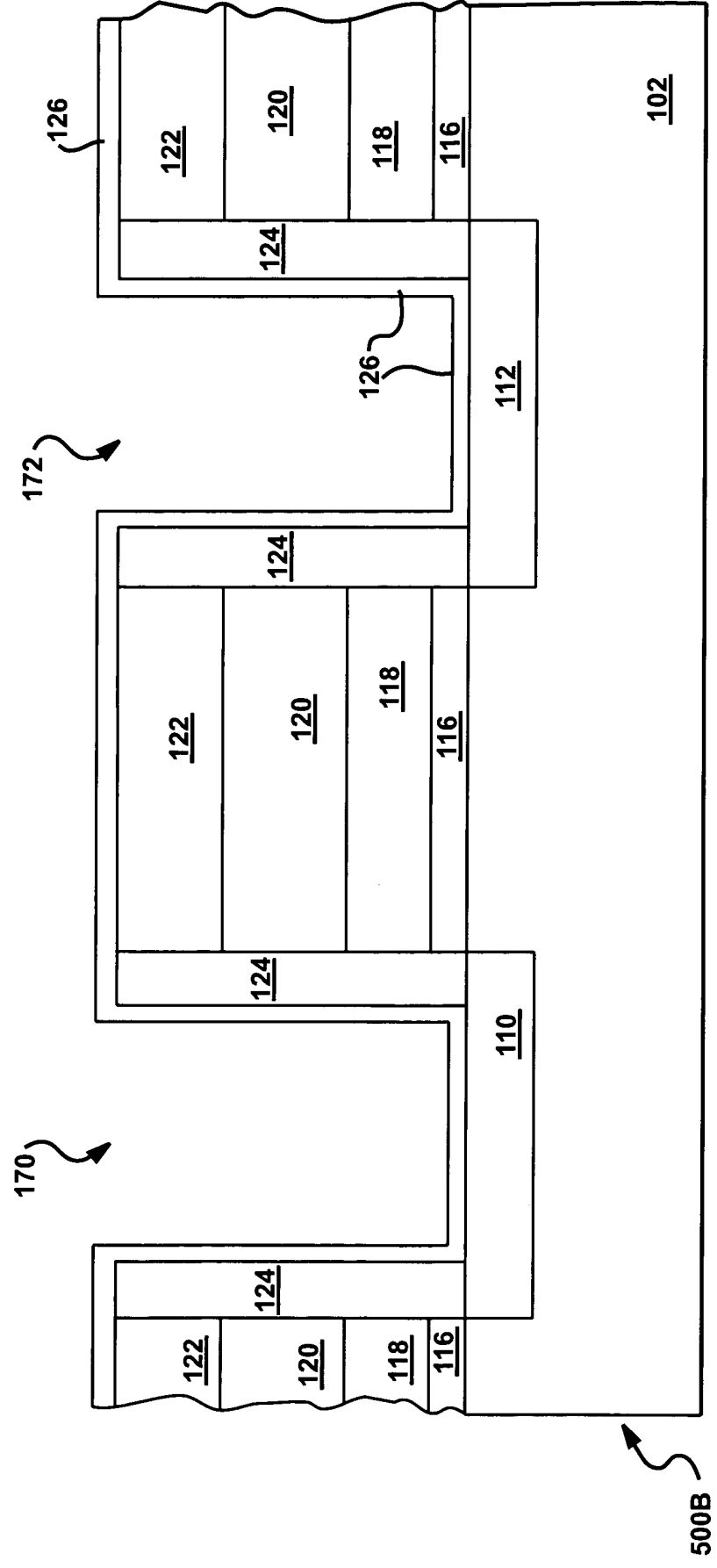
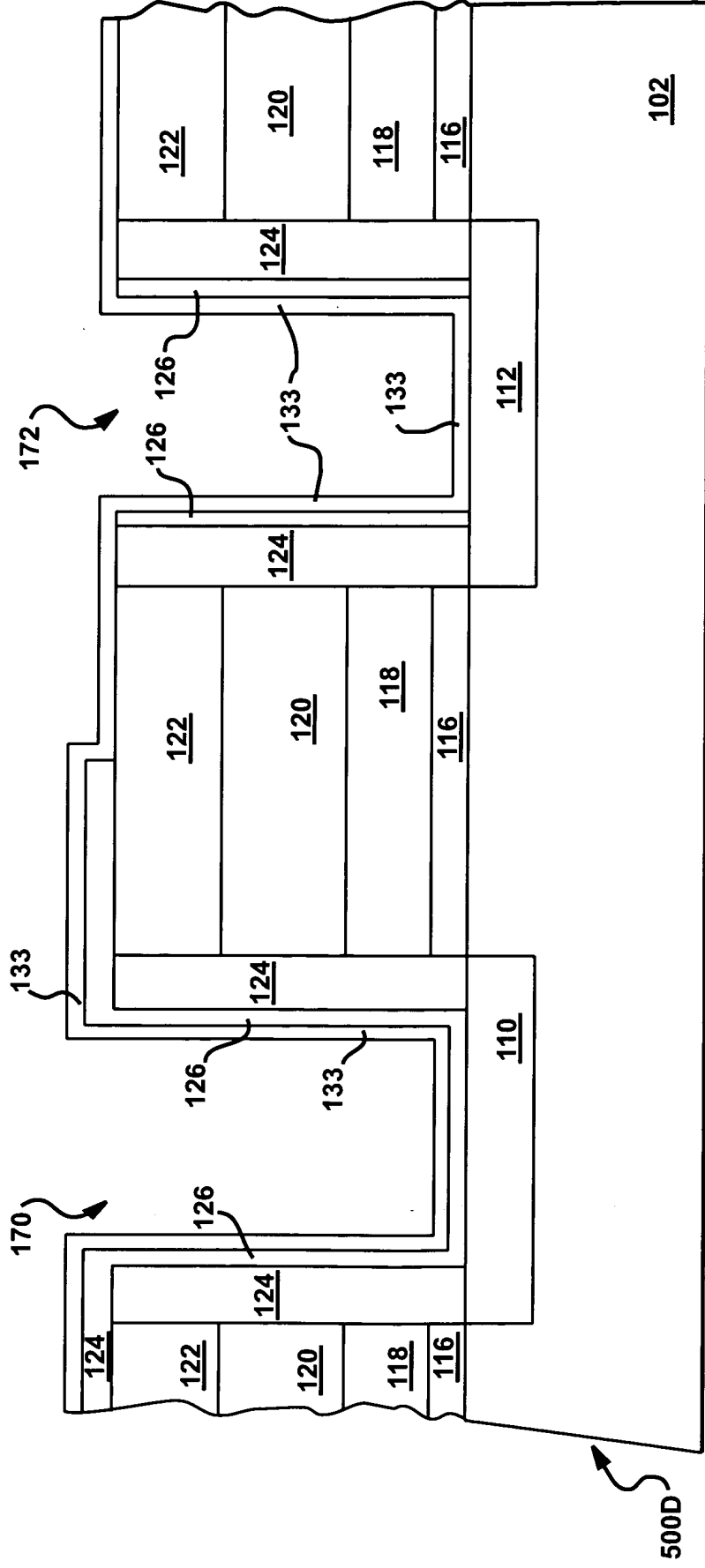


FIG - 5B



A cross-sectional view of a semiconductor device 500C. A mask is positioned above the device. Below the mask is a gate stack 110, 112. The gate stack 110, 112 is composed of a gate dielectric 124 and a gate conductive layer 126. The gate conductive layer 126 is divided into three regions: a first region 122, a second region 120, and a third region 118. The gate dielectric 124 is divided into four regions: a first region 126, a second region 124, a third region 126s, and a fourth region 126s. The gate stack 110, 112 is positioned over a substrate 102. The substrate 102 is divided into four regions: a first region 122, a second region 120, a third region 118, and a fourth region 116. The gate stack 110, 112 is positioned over the substrate 102. The gate stack 110, 112 is positioned over the substrate 102. The gate stack 110, 112 is positioned over the substrate 102.

500C

[illegible]

500E

500E

500F

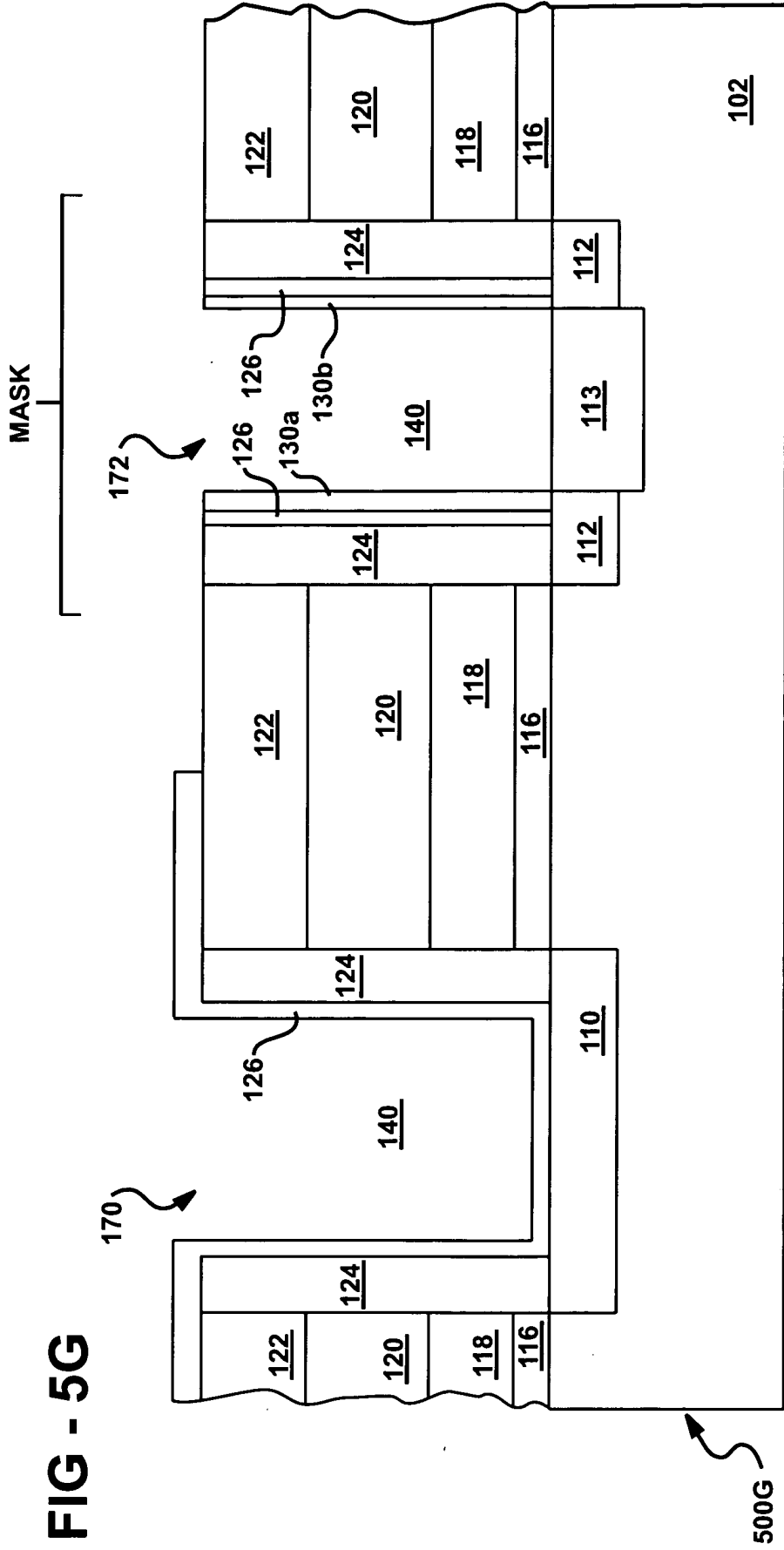
[illegible]

FIG - 5I

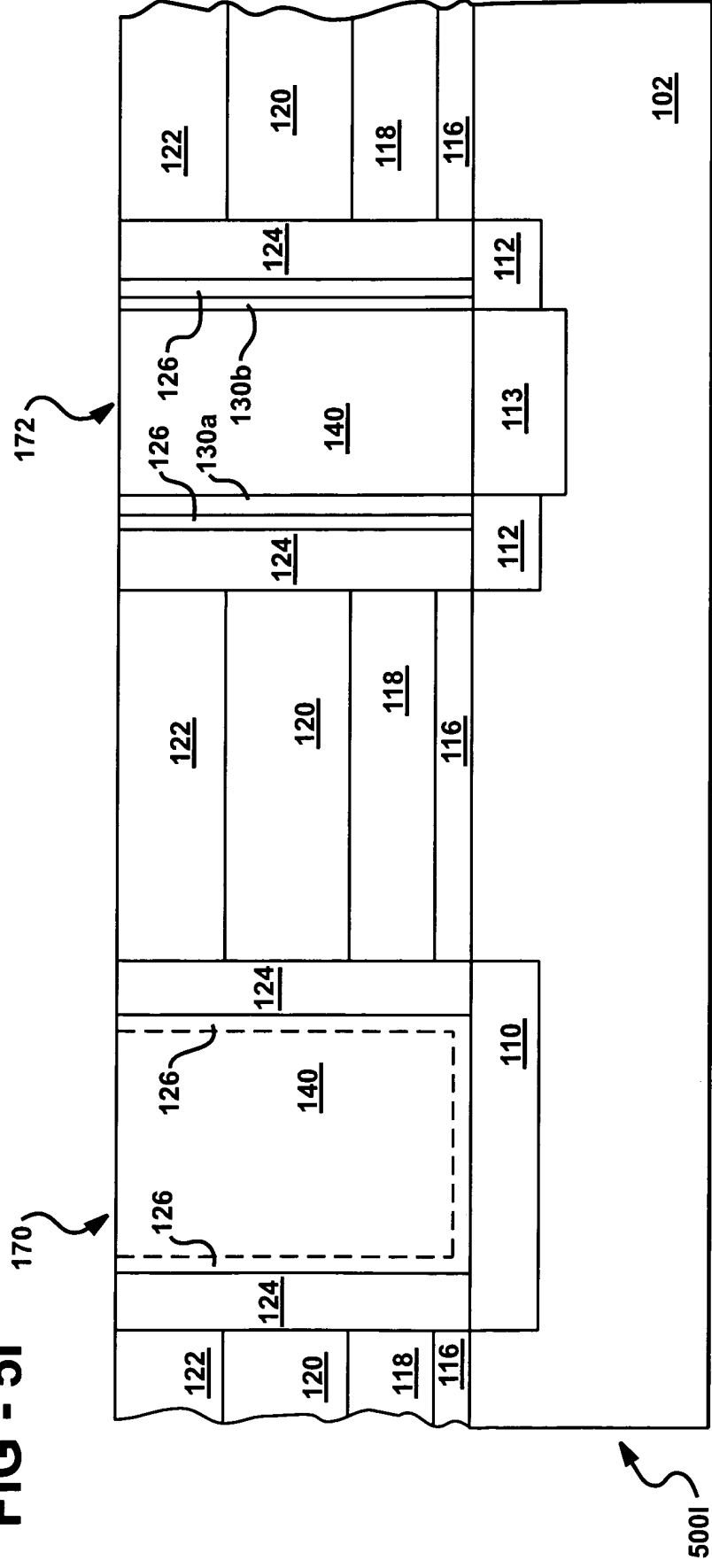


FIG - 5J

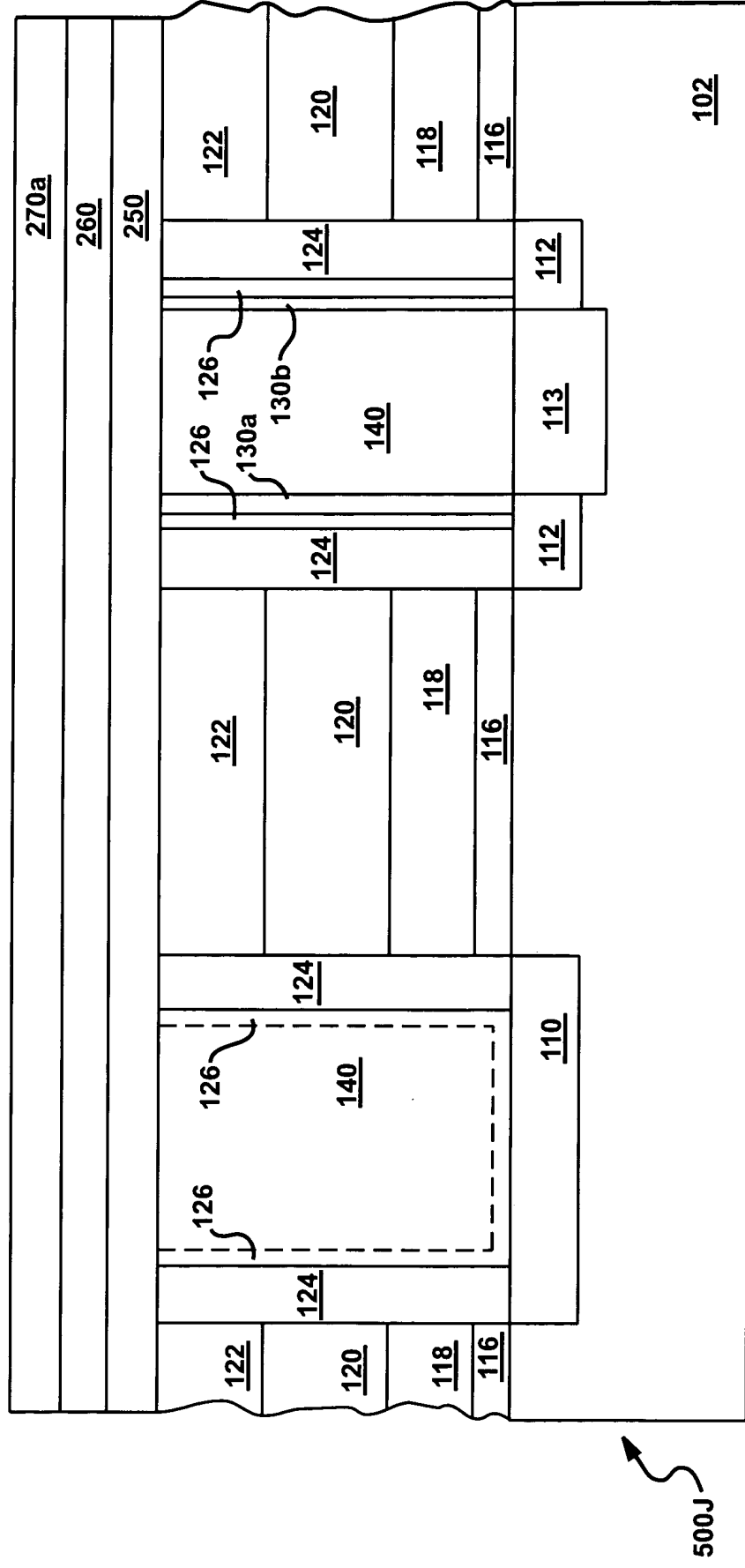


FIG - 5K

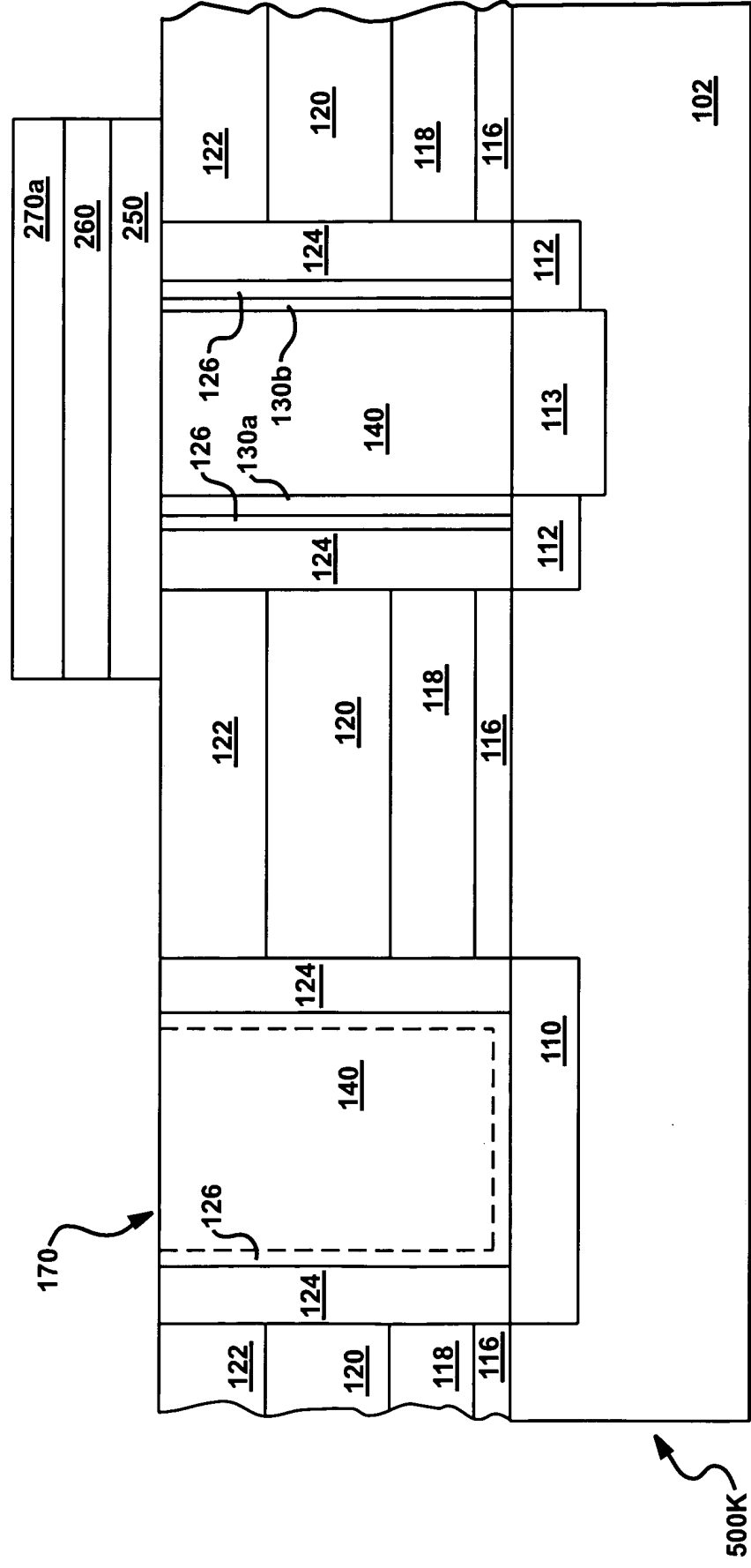
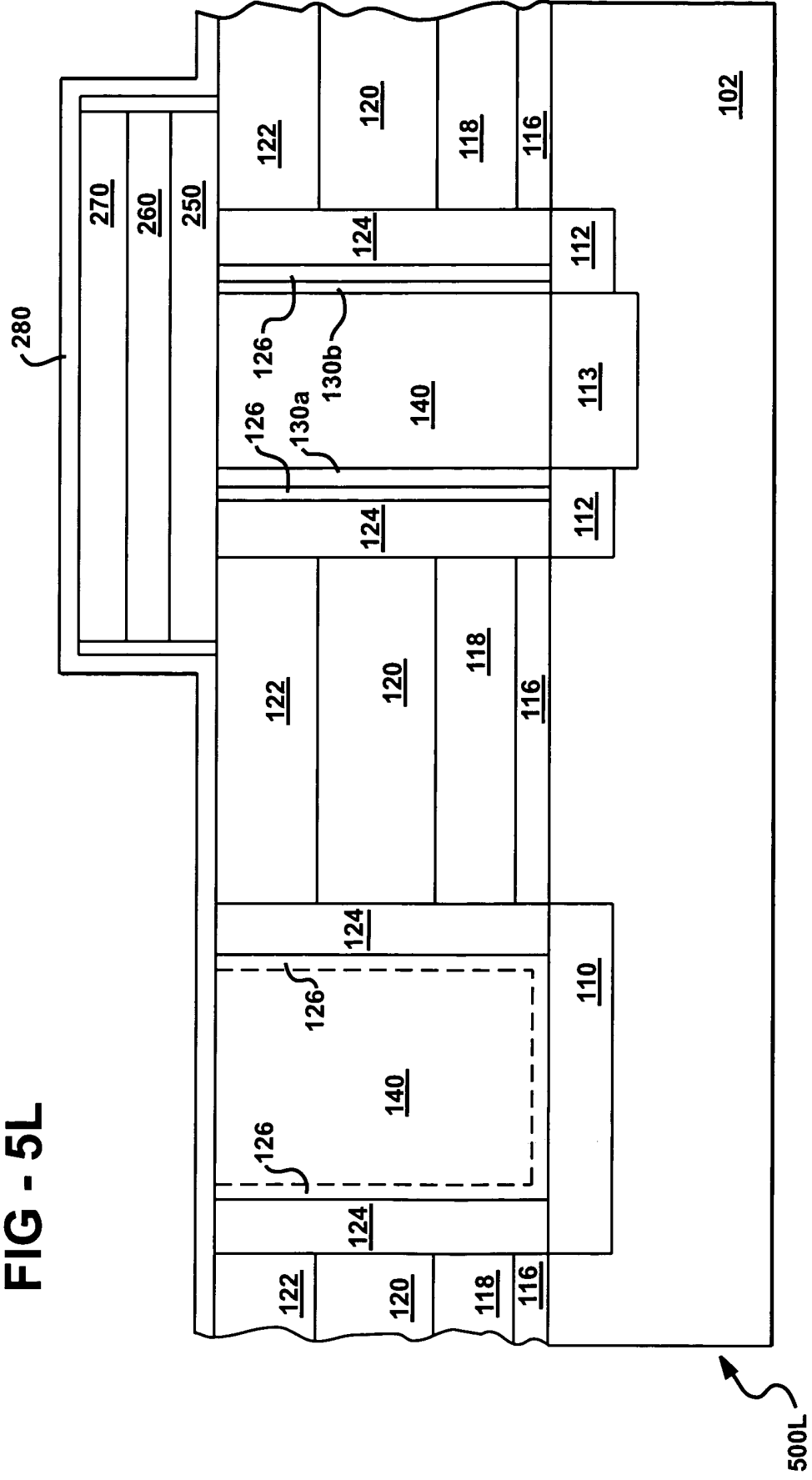


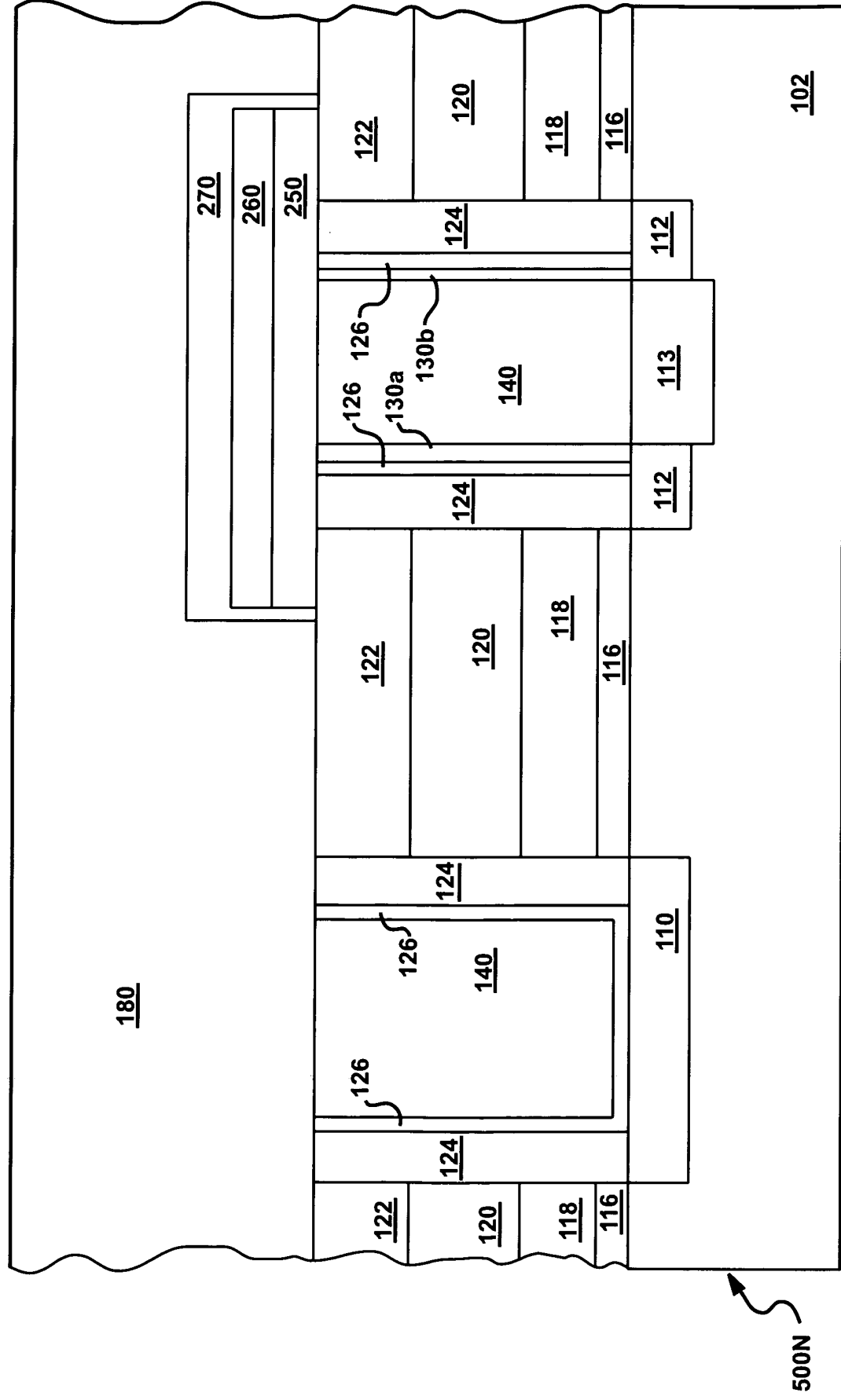
FIG - 5L



The diagram illustrates a 500M memory array structure. It features a central array of memory cells (102) organized in rows and columns. The array is divided into four quadrants by a central horizontal and vertical line. The top-left quadrant contains cells 122, 120, 118, and 116. The top-right quadrant contains cells 122, 120, 118, and 116. The bottom-left quadrant contains cells 122, 120, 118, and 116. The bottom-right quadrant contains cells 122, 120, 118, and 116. The array is surrounded by a peripheral circuitry (102) which includes a word line driver (110) and a bit line driver (112). The peripheral circuitry is connected to the array via word lines (124) and bit lines (126). The array is also connected to a power supply (500M) via a power line (126). The array is further divided into four quadrants by a central horizontal and vertical line. The top-left quadrant contains cells 122, 120, 118, and 116. The top-right quadrant contains cells 122, 120, 118, and 116. The bottom-left quadrant contains cells 122, 120, 118, and 116. The bottom-right quadrant contains cells 122, 120, 118, and 116. The array is surrounded by a peripheral circuitry (102) which includes a word line driver (110) and a bit line driver (112). The peripheral circuitry is connected to the array via word lines (124) and bit lines (126). The array is also connected to a power supply (500M) via a power line (126).

500M

FIG - 5N



5000

FIG - 6

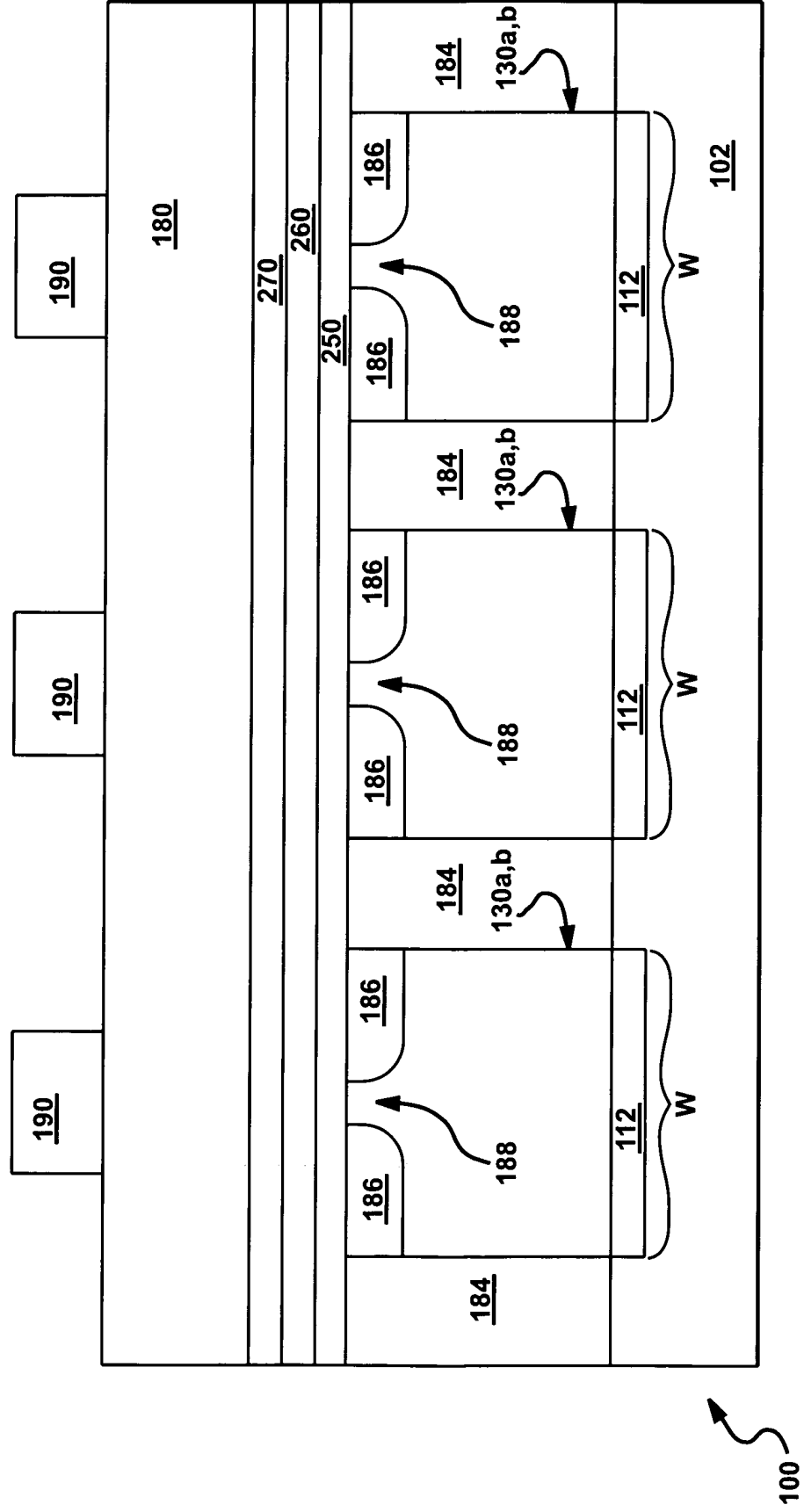


FIG - 7

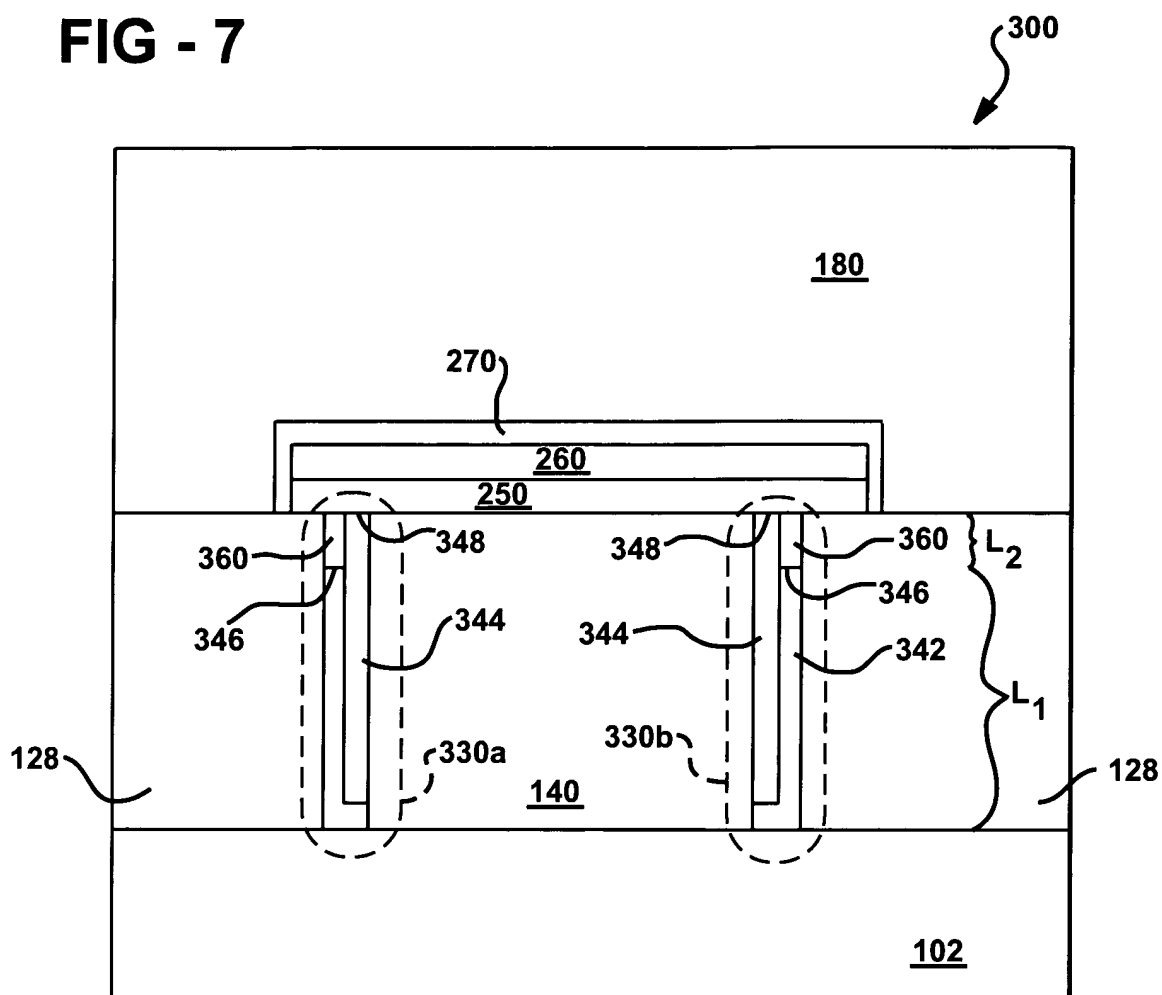


FIG - 8A

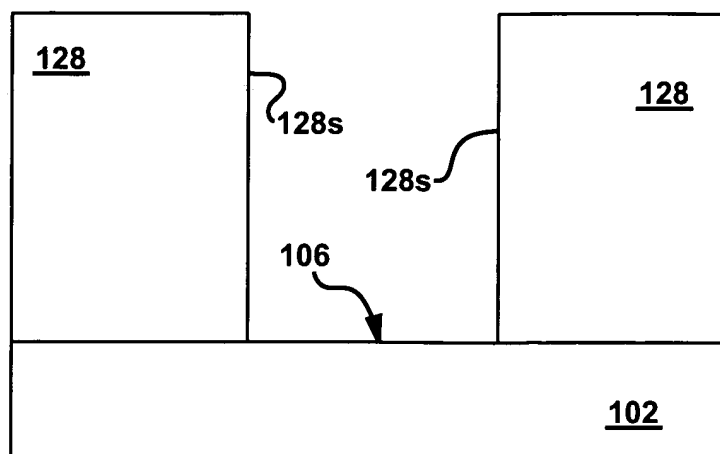


FIG - 8B

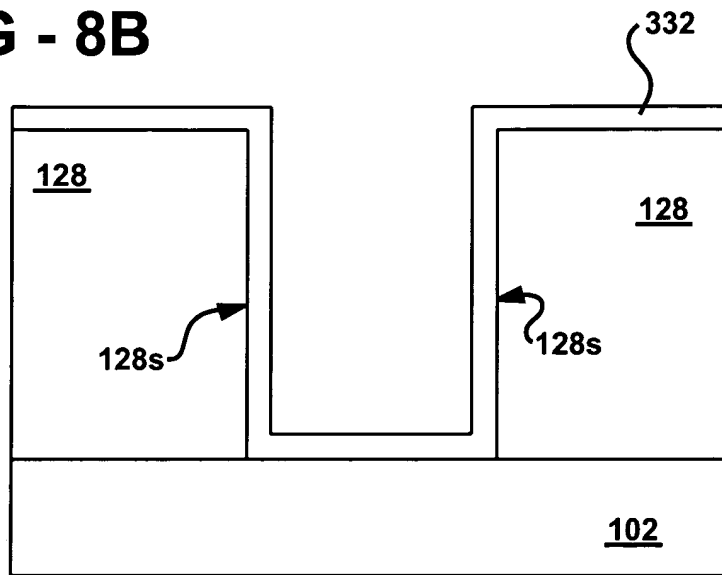


FIG - 8C

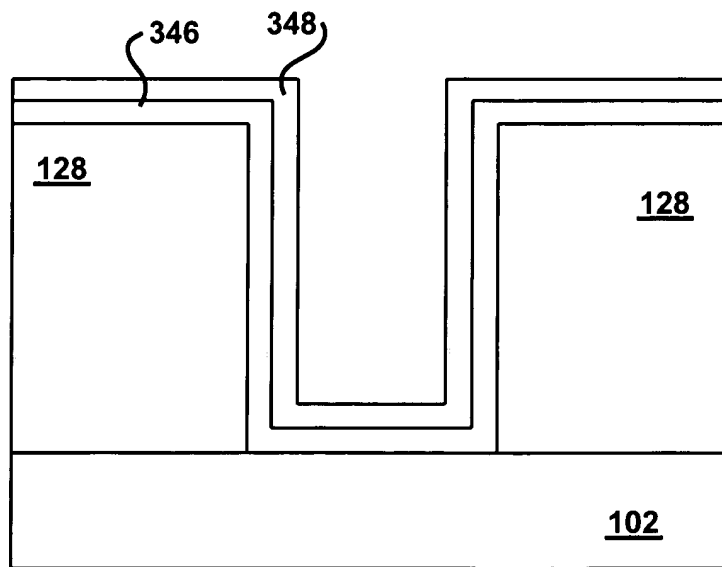


FIG - 8D

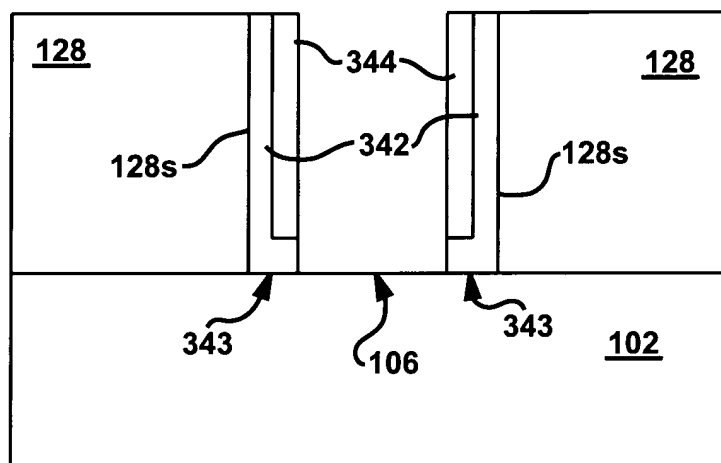


FIG - 8E

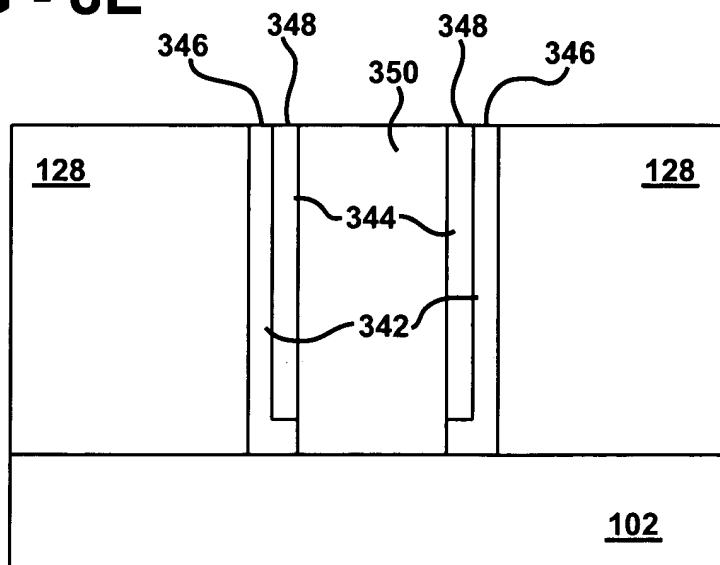


FIG - 9

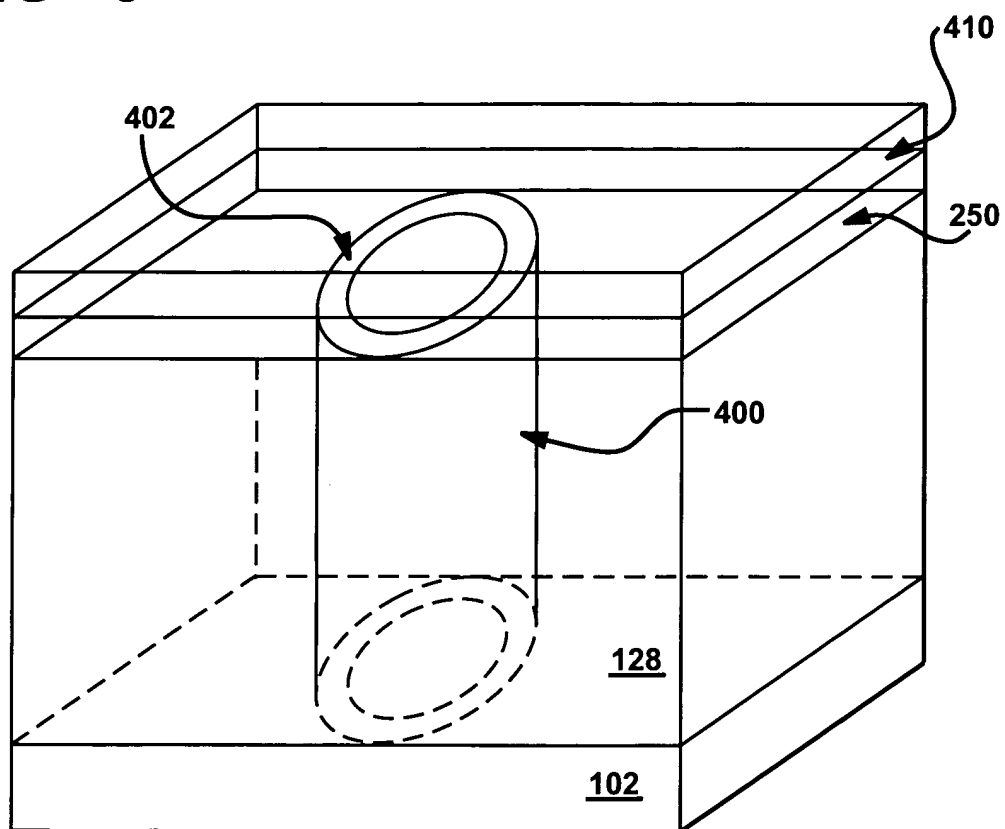


FIG - 10A

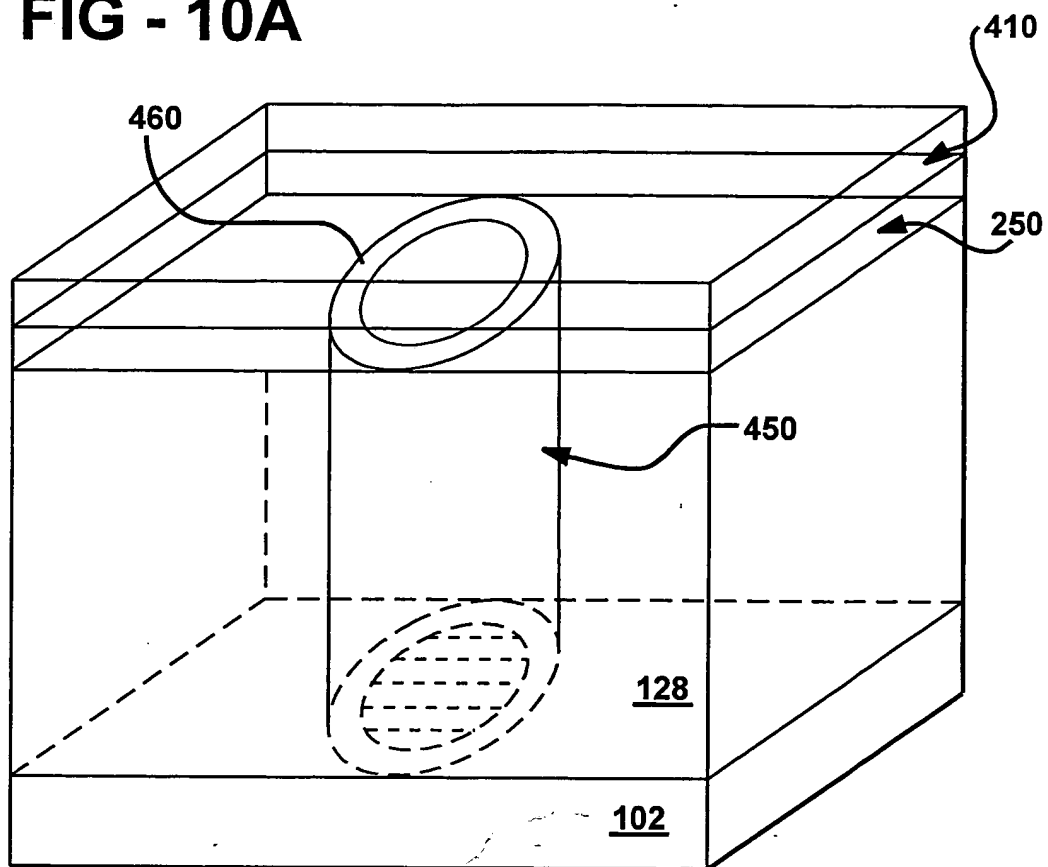


FIG - 10B

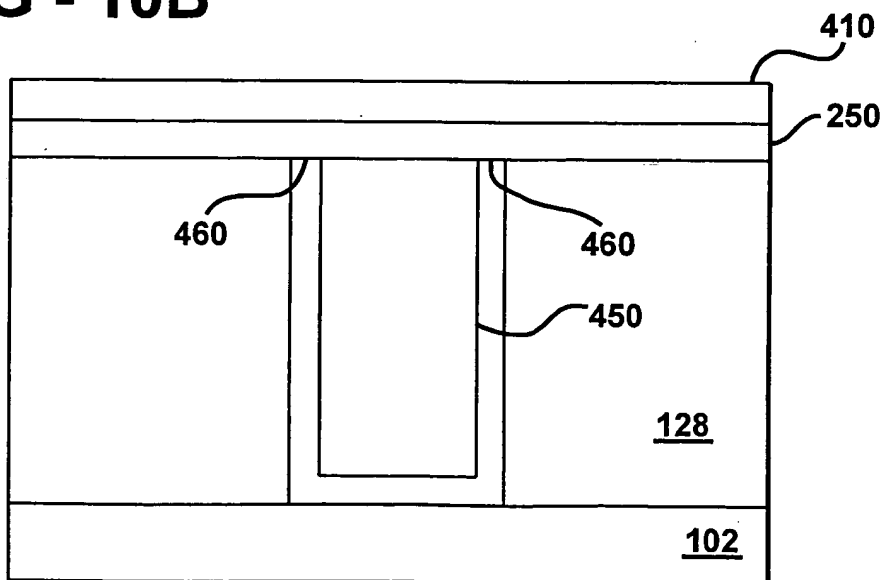


FIG - 11A

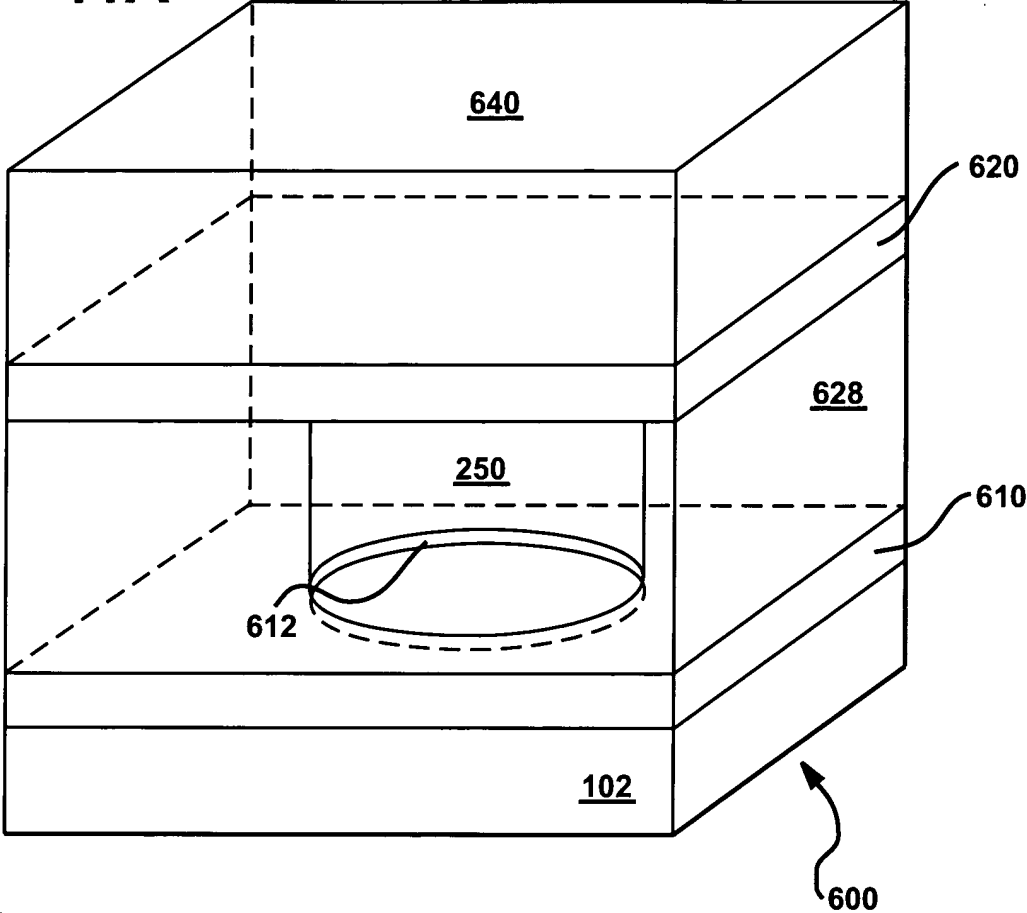


FIG - 11B

